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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,464	11/26/2003	Michael Byrne	T0461.70043 US00	8292

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EXAMINER
PATEL, NITIN C

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/04/2005

Steven J. Henry
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,464	BYRNE ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 November 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/23/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 28 are presented for examination.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because fig. 12 – 19 are not clean and it is difficult to read. . The drawings must be made on paper that has a white background (see 37 CFR 1.84 (e)). For example, drawings on graph paper, lined paper or paper that has a non-white background are not acceptable. See Figures 12 – 19.Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 23 June 2005 was filed before the mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

4. Claim 23, recites the limitation "ADC" on line 6, and ". The abbreviation of term "ADC" is required or defined at least once in claim.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5. Claims 17 – 18 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 17 - 18 of prior U.S. Patent No. 6,681,332 B1. This is a double patenting rejection.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1 – 16, and 19 – 28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 28 of U.S.

Patent No. 6,681,332 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

7. Claim 1 essentially repeats all the steps (a), (b), and (c) for placing the device in a selected mode of operation listed in the US. Pat. 6,681,332 B1, claim 1.

8. Claim 2 essentially repeats the step for placing the device select signal into an inactive logic state listed in the US. Pat. 6,681,332 B1, claim 2.

9. Claim 3 essentially repeats the inactive logic state as HIGH logic state listed in the US. Pat. 6,681,332 B1, claim 3.

10. Claim 4 essentially repeats the step of placing the device select signal into an active logic state listed in the US. Pat. 6,681,332 B1, claim 4.

11. Claim 5 essentially repeats the active logic state as LOW logic state listed in the US. Pat. 6,681,332 B1, claim 5.

12. Claim 6 essentially repeats the step for returning the device select signal to the first logic state after the occurrence of a first transition of the clock signal, but after the occurrence of a second subsequent transition of the clock signal listed in the US. Pat. 6,681,332 B1, claim 6.

13. Claim 7 essentially repeats the transition of the clock including the second falling edge of the clock signal that occurs after assertion of the device select signal in a second logic state listed in the US. Pat. 6,681,332 B1, claim 7.

14. Claim 8 essentially repeats the reduced power consumption mode, and second subsequent transition of the clock signal includes the tenth falling edge of the clock

signal that occurs after the assertion of device select signal in a second logic state listed in the US. Pat. 6,681,332 B1, claim 8, and 1.

15. Claim 9 essentially repeats the steps (d), and (e) for restoring the device in a normal operating mode listed in the US. Pat. 6,681,332 B1, claim 1.

16. Claim 10 essentially repeats the second user-controlled time window defined by at least ten falling edges of the clock signal listed in the US. Pat. 6,681,332 B1, claim 7.

17. Claim 11 essentially repeats all the steps (a), (b), and (c) for placing the integrated circuit device having a chip select [CS] input and a clock [CLK] input into a selected mode of operation listed in the US. Pat. 6,681,332 B1, claim 11.

18. Claim 12 essentially repeats the initial inactive logic state as HIGH logic state listed in the US. Pat. 6,681,332 B1, claim 12.

19. Claim 13 essentially repeats the initial active logic state as LOW logic state listed in the US. Pat. 6,681,332 B1, claim 13.

20. Claim 14 essentially repeats the reduced power consumption mode, and second subsequent transition of the clock signal includes the tenth falling edge of the clock signal that occurs while the CS is in the active logic state listed in the US. Pat. 6,681,332 B1, claim 14, and 11.

21. Claim 15 essentially repeats the steps (d), and (e) for restoring the device in a normal operating mode listed in the US. Pat. 6,681,332 B1, claim 15.

22. Claim 16 essentially repeats the second user-controlled time window defined by at least ten falling edges of the clock signal listed in the US. Pat. 6,681,332 B1, claim 16.

23. Claim 19 essentially repeats the means for changing operating mode of the device places the device in a first selected mode of operation in response to a first combination of logic state transitions, and places the device in a second selected mode of operation in response to a second combination of logic state transitions listed in the US. Pat. 6,681,332 B1, claim 19.

24. Claim 20 essentially repeats the state transitions at the clock input, occurring between logic state transitions at the device select input listed in the US. Pat. 6,681,332 B1, claim 20.

25. Claim 21 essentially repeats the second combination of logic state transitions further includes at least ten logic state transitions the clock input, occurring between logic state transitions at the device select input listed in the US. Pat. 6,681,332 B1, claim 21.

26. Claim 22 essentially repeats an analog-to-digital converter with all the means for converting an analog input signal into a corresponding digital signal; means for outputting the corresponding digital signal in serial form; means for generating at least one command signal in response to a number of serial clock signal cycles occurring between changing states of the control signal; and means for selecting an operating mode of the analog-to- digital converter in response to the command signal listed in the US. Pat. 6,681,332 B1, claim 22.

27. Claim 23 essentially repeats the means for converting an analog input signal into a corresponding digital signal further includes a track and hold circuit coupled to the

analog input signal; and a successive approximation ADC coupled to the track and hold circuit. listed in the US. Pat. 6,681,332 B1, claim 23.

28. Claim 24 essentially repeats the means for outputting a corresponding digital signal further includes a data multiplexer coupled to said means for converting the analog input signal and to said serial clock signal; and a serial data output coupled to the data multiplexer listed in the US. Pat. 6,681,332 B1, claim 24.

29. Claim 25 essentially repeats the means for generating at least one command signal further includes clock divider and counter logic coupled to the serial clock signal and the control signal, wherein the clock divider and counter logic generates a plurality of command signals conditioned, at least in part, by the number of serial clock signal cycles occurring between changing states of the control signal listed in the US. Pat. 6,681,332 B1, claim 25.

30. Claim 26 essentially repeats the means for means for selecting an operating mode of the analog-to-digital converter in response to the command signal further comprises control and power management logic coupled to the control signal and the clock divider and counter logic listed in the US. Pat. 6,681,332 B1, claim 26.

31. Claim 27 essentially repeats the integrated circuit subsystem with interconnection arrangement of devices and control circuit [control and power management logic with clock divide and Johnson counter] coupled to the device select and serial clock input signals, to place plurality of integrated circuits into DAISY CHAIN mode of operation in response to user-controlled number of logic state transitions of serial clock input signal

occurring between logic state transitions of the device select signal listed in the US. Pat. 6,681,332 B1, claim 11, and 22.

32. Claim 28 essentially repeats an analog-to-digital converter with the conversion subsystem that convert an analog input signal into digital signal; a device select signal and serial clock input signal; a range programming subsystem [means for applying power with power management logic coupled to control signal and clock divider] responsive to device select and clock such that such that full-scale input voltage ranges in response to user controlled number of logic state transitions of serial input clock occurring between logic state transition of the device select signal listed in the US. Pat. 6,681,332 B1, claims 22, and 26.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

33. Claims 1 – 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schreiber et al. [hereinafter as Schreiber], US Patent 6,456,219 B1, and further in view of Suzuki, US Patent 6,057,795.

34. As to claims 1, 11, 17, and 22 Schreiber teaches a device and method for placing a device [analog-to-digital converter] in a selected mode of operation including initializing a device select signal [SCLK] into a first logic [level "1"] state [col. 6, lines 14 – 23]; asserting the device select signal [SCLK] in a second logic [level "0"] state [col. 6, lines 24 – 25]; and returning the device select signal [SCLK] to the first logic [level "1"] state with time period [conversion cycle/period] [col. 3, lines 35 – 43, col. 4, lines 39 – 67, col. 5, 1 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 11, col. 9, lines 11 – 26, fig. 1].

However, Schreiber does not teach explicitly that the state transition time period [time window] for returning the select signal in first state is user–controlled.

Suzuki teaches an analog-to-digital [A/D] converter, a mode selection section for selecting a conversion mode and a standby mode, and control section for controlling A/D based on the respective mode and breaks the current path during a standby mode [first state] and duration [time window] specified from outside of the system [user-controlled][col. 1, lines 48 – 57, col. 3, lines 7 – 53, col. 4, lines 34 – 52].

It would have been obvious to one of ordinary skill in art, having the teachings of Schreiber and Suzuki before him at the time of invention was made, to modify the controller [107] and timing generator [17] disclosed by Schreiber to include a capability of specifying the duration from outside [user-controlled/specified] as taught by Suzuki in order to obtain an analog-to-digital converter [A/D device] and method of operation with

duration of standby mode specified from outside [user-controlled] to obtain an optimum periodic or intermittent operation of system while saving power, and a variable setting for standby counter enables a single clock signal to control different timings in system thereby avoiding an increase of the size [col. 4, lines 35 – 46].

35. As to claim 27, Schreiber teaches an integrated circuit subsystem [col. 1, lines 6 – 8] comprising: a plurality of integrated circuit devices each having a signal input and a signal output, the devices interconnected such that a signal output of a preceding device is coupled to a signal input of a subsequent device, and the integrated circuit devices share common device select and serial clock input signals; and control circuitry coupled to the device select and serial clock input signals, the control circuitry placing the plurality of integrated circuits into a DAISY CHAIN mode of [sequential] operation in response to a number of logic state transitions of the serial clock input signal occurring between logic state transitions of the device select signal [col. 3, lines 35 – 43, col. 4, lines 39 – 67, col. 5, 1 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 11, col. 9, lines 11 – 26, fig. 1 – 8].

However, Schreiber does not teach explicitly that the number of state transitions occurring between logic state transition of device select signal is user–controlled.

Suzuki teaches an analog-to-digital [A/D] converter, a mode selection section for selecting a conversion mode and a standby mode, and control section for controlling A/D based on the respective mode and breaks the current path during a standby mode [first state] and duration [time window] specified from outside of the system [user-controlled][col. 1, lines 48 – 57, col. 3, lines 7 – 53, col. 4, lines 34 – 52].

It would have been obvious to one of ordinary skill in art, having the teachings of Schreiber and Suzuki before him at the time of invention was made, to modify the controller [107] and timing generator [17] disclosed by Schreiber to include a capability of specifying the duration from outside [user-controlled/specified] as taught by Suzuki in order to obtain an analog-to-digital converter [A/D device] and method of operation with duration of standby mode specified from outside [user-controlled] to obtain an optimum periodic or intermittent operation of system while saving power, and a variable setting for standby counter enables a single clock signal to control different timings in system thereby avoiding an increase of the size [col. 4, lines 35 – 46].

36. As to claim 28, Schreiber teaches an analog-to-digital converter having an analog input signal [Vin, col. 2, line 15] and digital output signal [Dout, fig. 1] comprising: a conversion subsystem [100, fig. 1] that converts the analog input signal [Vin] into the digital output signal [Dout][col. 4, lines 38 – 52]; a range programming subsystem responsive to a device select input signal and a serial clock input signal; such that full-scale input voltage range [internal reference voltages] of the analog- to-digital converter is selected from among a plurality of full-scale input voltage ranges [col. 9, lines 20 – 26] in response to a number of logic state transitions of the serial clock input signal occurring between logic state transitions of the device select signal [col. 3, lines 44 – 64, col. 8, lines 38 – 43, col. 9, lines 11 – 26].

However, Schreiber does not teach explicitly that the number of logic state transition of the serial clock is user–controlled.

Suzuki teaches an analog-to-digital [A/D] converter, a mode selection section for selecting a conversion mode and a standby mode, and control section for controlling A/D based on the respective mode and breaks the current path during a standby mode [first state] and duration [time window] specified from outside of the system [user-controlled][col. 1, lines 48 – 57, col. 3, lines 7 – 53, col. 4, lines 34 – 52].

It would have been obvious to one of ordinary skill in art, having the teachings of Schreiber and Suzuki before him at the time of invention was made, to modify the controller [107] and timing generator [17] disclosed by Schreiber to include a capability of specifying the duration from outside [user-controlled/specified] as taught by Suzuki in order to obtain an analog-to-digital converter [A/D device] and method of operation with duration of standby mode specified from outside [user-controlled] to obtain an optimum periodic or intermittent operation of system while saving power, and a variable setting for standby counter enables a single clock signal to control different timings in system thereby avoiding an increase of the size [col. 4, lines 35 – 46].

37. As to claims 2 – 3, 12, Schreiber teaches an initializing [reset] a device select signal [SCLK], and placing the device select signal [SCLK] into an inactive logic state, which is a HIGH logic [logic "1"] state [col. Col. 6, lines 14 – 18].

38. As to claims 4 – 5, 13, 15, Schreiber teaches an asserting the device select signal [SCLK] and placing the device select signal [SCLK] into an active logic state, which is a LOW logic [logic "0"] state [col. 6, lines 24 – 25].

39. As to claims 6 – 10, Suzuki teaches generating a timing signals with timing diagram representing clock, start, stop signal, standby signal [fig. 6].

40. As to claim 14, Schreiber discloses reduced power consumption mode [power down operation] [col. 6, lines 32 – 41, fig. 8].

41. As to claim 18 – 21, Suzuki teaches clock signal [CLOCK], timing signal with standby counter [27, fig. 5] to activate and inactivate standby state signal [fig. 5] by counting the number of pulses of clock to reestablish condition necessary for to start new conversion [col. 3, lines 7 – 15].

42. As to claim 23, Schreiber discloses an analog-to-digital converter and method of operation which teaches successive approximation [col. 10, lines 36 – 40], and track and hold circuit is inherent to converter core moreover, is also very well known in A/D converter [please also refer Fong, US Patent 5,367,300] too.

43. As to claim 24, Schreiber teaches a data multiplexer [23, MUX] coupled to means of converter and serial clock signal [SCLK], and a serial data output [Dout] [fig. 2, 3, 6].

44. As to claim 25, Schreiber discloses the analog-to-digital converter including a means for generating [DSP] at least one command [col. 6, lines 14 – 41, col. 7, lines 60 – 67, col. 8, lines 1 - 30], command register [25], counter [16, timer] and a controller [107] command register [25] coupled with timing generator [17], therefore he teaches necessary clock divider too [col. 44 – 63, col. 7, lines 60 – 67, col. 8, lines 1 – 30, fig. 5 – 6, fig. 1,3,6].

45. As to claim 26, Schreiber discloses the analog-to-digital converter including a means for selecting [107, controller] an operating mode [Power Down] in response to command signal [25, command register] including power management logic [selecting values of internal values], counter [16, timer] logic, and timing generator [17] [col. 6,

lines 33 – 41, col. 7, lines 60 – 67, col. 8, lines 1 – 30, col. 9, lines 11 – 26], and a controller [107] coupled with timing generator [17] therefore, he teaches necessary clock divider too [col. 44 – 63, col. 7, lines 60 – 67, col. 8, lines 1 – 30, fig. 5 – 6].

46. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

47. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
July 26, 2005

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